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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/605,092 | 09/08/2003 | Satoshi Kitamura | SIC-03-035 | 2091 |

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| EXAMINER | |
|---|---|
| PARRIES, DRU M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2836 | |

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/605,092 | KITAMURA ET AL. | |
| | Examiner | Art Unit | |
| | Dru M. Parries | 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-8-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claims 32, 35 and 36 are objected to because of the following informalities: They lack antecedent basis ("*the* first split second" and "*the* second split second") or they claim dependency to the wrong claim. Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 13-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakabayashi et al. (JP 04-150729 A) and Mitchell (6,355,990). Regarding claim 1, Nakabayashi teaches first and second storage elements (12, 13) receiving power from an AC power supply (8) (Fig. 3). Nakabayashi fails to teach the storage elements supplying power to two different electrical components. Mitchell teaches two storage elements that provide power to two different electrical components (R1, R2). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the storage elements supply power to different components because it allows for more precise control over the system and have it work more efficiently.

Regarding claims 2 and 3, Nakabayashi doesn't teach a power inhibiting unit structured to prevent power from being transferred from the first storage element to the second electrical component and vice versa. Mitchell teaches a power inhibiting structure to prevent power from

being transferred from first storage to second electrical component and vice versa (Fig. 1A and 6). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this structure into Nakabayashi's invention so that the correct amount of power will be provided into each load and there is no risk for overvoltage or burn out.

Regarding claims 4, 5, 13-22, Nakabayashi teaches a rectifier circuit (9) which converts and stabilizes the AC current to DC current and is coupled to first and second storage elements. He also teaches the first and second storage elements to receive current in parallel. He teaches a reverse current inhibiting unit that comprises diodes (15) between the rectifier circuit and the first and second storage elements. Nakabayashi also teaches a power switch unit (14), included in the reverse current inhibiting unit, which selectively switches current from rectifier circuit to at least one of first or second storage element. (Abstract; Figs. 2 & 3) Nakabayashi fails to teach the power switch unit comprising first and second switch circuits to selectively switch current from rectifier to first and second storage elements in response to the voltage at the first and second storage elements. Mitchell teaches first and second switch circuits (S1, S2) that selectively switch current to the first and second storage elements based on the voltage at the first and second storage elements (Col. 1, lines 60-67). It would have been obvious to one of ordinary skill in the art at the time of the invention to selectively switch current to the storage elements so that the correct amount of voltage is supplied to each load and thereby enhance efficiency.

4. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakabayashi et al. (JP 04-150729 A) and Mitchell (6,355,990) as applied to claims 1, 4 and 5 above, and further in view of Flory, IV (6,388,392). Nakabayashi and Mitchell teach a power supply system as described above. Mitchell also teaches a power switch unit (S1) that selectively switches

current from the rectifier circuit to the first storage element (C1) in response to the voltage of the first storage element. They both fail to teach power flowing from the first storage element to the second storage element through diodes. Flory, IV teaches current that flows from the first storage element (ESB of 70a) to the second storage element (ESB of 70b) via a diode (62 of 70b). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate this circuit design into Nakabayashi's invention so that when the first storage element is fully charged it can pass the excess charge onto the second storage element so no charge will be wasted thereby making the system more efficient.

5. Claims 10-12, and 23-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakabayashi et al. (JP 04-150729 A), Mitchell (6,355,990) and Flory, IV (6,388,392) as applied to claims 1, 4-7, 13, and 16 above, and further in view of Turner (2002/0014366). Nakabayashi, Mitchell and Flory teach a power supply system as described above. Nakabayashi also teaches diodes between all switch units and storage elements. Mitchell also teaches the idea of having a plurality of energy storage units to provide power to a plurality of electrical components (abstract, lines 10-16) and the idea of a power switch unit (Sn) that selectively switches current to the nth storage element (Cn) in response to the voltage of the nth storage element. Therefore, Mitchell teaches a first split first storage element (Cn) and second split first storage element (C(n+1)) (same with first and second split second storage elements). The three above references fail to explicitly teach the type of electrical components being powered. Turner teaches the type of electrical components being that of a bicycle. Turner teaches a first electrical component being a mechanical adjusting mechanism (166, 168) (i.e. transmission or suspension) and a second electrical component being a microprocessor (150) and/or a sensor element (184), which

has a lower capacitance than the first electrical component. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate these electrical components as the loads of Nakabayashi's power system because the type of load wasn't explicitly taught and these loads are known in the art and would create a more efficient bicycle power system.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dru M. Parries whose telephone number is (571) 272-8542. The examiner can normally be reached on Monday -Thursday from 8:00am to 5:00pm. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus, can be reached on 571-272-2800 x 36. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMP

10-4-2005

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